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Embedded system architectures for artificial neural networks

Embedded Systems, artificial neural network, neurochips



This project concerns a comprehensive overview of the hardware realizations of artificial neural network (ANN) models, known as hardware neural networks (HNN), appearing in academic studies as prototypes as well as in commercial use. HNN research has witnessed a steady progress while the commercial adoption of the technology has evolved at a slower pace. The project aims to explore the progress in the ANN/HNN field including its models, hardware mapped design approaches, and related applications. Hence the aim here is to study several and as many as possible of the ANN modules, research and build suitable hardware architectures to run these modules and perform study cases using a wide range of illustrative applications and examples. On a lower level, the chip design approaches, whether it was analog, digital or hybrid, at neuronal level and as neurochips realizing complete ANN models are studied.

The project discuss, in details, neuromorphic designs such as spiking neural network hardware, cellular neural network implementations and their mapping on reconfigurable FPGA based implementations, in particular, for stochastic ANN models, and optical implementations. Parallel digital implementations employing bit-slice, systolic, and SIMD architectures, implementations for associative neural memories, and RAM based implementations are also outlined. We trace the recent trends and explore potential future research directions.

Source: <http://www.sciencedirect.com/science/article/pii/S092523121000216X>